CLAIMS

[1] A semiconductor integrated circuit, comprising:

first and second information holding circuits formed in a memory cell array for holding information;

a first port section for inputting or outputting information, which is connected only to the first information holding circuit;

a second port section for inputting or outputting information, which is connected only to the second information holding circuit; and

an interchange circuit receiving an interchange control signal for interchanging, in the memory cell array, information held in the first information holding circuit and information held in the second information holding circuit with each other.

[2] The semiconductor integrated circuit of claim 1, wherein:

the first and second port sections are each formed by a transistor circuit; and

the transistor circuit of the first port section is formed by transistors of a threshold voltage and the transistor circuit of the second port section is formed by transistors of a different threshold voltage.

[3] The semiconductor integrated circuit of claim 2, wherein:

an access frequency of the first port section and that of the second port section are different from each other; and

the access frequency of the port section formed by transistors of a higher threshold voltage is lower than that of the port section formed by transistors of a lower threshold voltage.

[4] The semiconductor integrated circuit of claim 1, wherein a power source voltage supplied to the first port section and that supplied to the second port section are different from each other.

[5] The semiconductor integrated circuit of claim 4, wherein an access frequency

of the port section of a lower power source voltage is lower than that of the port section of a higher power source voltage.

[6] The semiconductor integrated circuit of claim 1, wherein:

the first and second information holding circuits are each formed by a transistor circuit; and

the transistor circuit of the first information holding circuit is formed by transistors of a threshold voltage and the transistor circuit of the second information holding circuit is formed by transistors of a different threshold voltage.

[7] The semiconductor integrated circuit of claim 6, wherein an access frequency of the information holding circuit formed by transistors of a higher threshold voltage is lower than that of the information holding circuit formed by transistors of a lower threshold voltage.

[8] The semiconductor integrated circuit of claim 1, wherein a power source voltage supplied to the first information holding circuit and that supplied to the second information holding circuit are different from each other.

[9] The semiconductor integrated circuit of claim 8, wherein an access frequency of the information holding circuit of a lower power source voltage is lower than that of the information holding circuit of a higher power source voltage.

[10] The semiconductor integrated circuit of claim 1, wherein:

the interchange circuit includes a temporary holding circuit for temporarily holding information; and

information held in the first information holding circuit and information held in the second information holding circuit are interchanged with each other via the temporary holding circuit based on the interchange control signal.

[11] The semiconductor integrated circuit of claim 1, wherein a completion of an interchange operation in which information held in the first information holding circuit and

information held in the second information holding circuit are interchanged with each other is detected, upon which an output of the interchange control signal is stopped.

[12] The semiconductor integrated circuit of claim 1, wherein a completion of an operation in which information that should be held in the first and second information holding circuits are held in the first and second information holding circuits is detected, after which the information held in the first information holding circuit and the information held in the second information holding circuit are interchanged with each other.

[13] The semiconductor integrated circuit of claim 1, wherein:

the first and second port sections are each formed by a transistor circuit;

each of the transistor circuits of the first and second port sections is formed by transistors of a transistor width according to an access speed of the port section; and

the transistor width of the transistor circuit of the port section of a lower access speed is smaller than that of the transistor circuit of the port section of a higher access speed.

[14] The semiconductor integrated circuit of claim 1, wherein:

the first and second information holding circuits are each formed by a transistor circuit;

each of the transistor circuits of the first and second information holding circuits is formed by transistors of a transistor width according to an access speed of the port section that is connected to the information holding circuit; and

the transistor width of the transistor circuit of the information holding circuit of a lower access speed is smaller than that of the transistor circuit of the information holding circuit of a higher access speed.

[15] The semiconductor integrated circuit of claim 10, wherein the temporary holding circuit is formed by a latch circuit.

[16] The semiconductor integrated circuit of claim 15, wherein the latch circuit is a

differential circuit.

[17] The semiconductor integrated circuit of claim 8, wherein the interchange circuit includes a latch circuit for temporarily holding information held in the information holding circuit of a lower power source voltage and outputting the held information to the information holding circuit of a higher power source voltage.

[18] The semiconductor integrated circuit of claim 1, wherein:

the first and second port sections and the first and second information holding circuits are each formed by a transistor circuit;

a group including the first port section and the first information holding circuit and a group including the second port section and the second information holding circuit each include a substrate voltage control circuit; and

the substrate voltage control circuit of each group controls a threshold voltage of transistors forming the transistor circuits of the port section and the information holding circuit of the group to a threshold voltage according to an access frequency of the port section of the group.

[19] The semiconductor integrated circuit of claim 1, wherein:

a group including the first port section and the first information holding circuit and a group including the second port section and the second information holding circuit each include a power source voltage control circuit; and

the power source voltage control circuit of each group controls a power source voltage supplied to the port section and the information holding circuit of the group according to an information read time and an information write time for the port section of the group.

[20] The semiconductor integrated circuit of claim 1, wherein:

the first and second port sections and the first and second information holding circuits are each formed by a transistor circuit;

a group including the first port section and the first information holding circuit and a group including the second port section and the second information holding circuit each include a substrate voltage control circuit and a power source voltage control circuit;

the substrate voltage control circuit of each group controls a threshold voltage of transistors of the transistor circuits of the port section and the information holding circuit of the group to a predetermined threshold voltage; and

the power source voltage control circuit of each group controls a power source voltage supplied to the port section and the information holding circuit of the group so as to control an information read time and an information write time for the port section of the group to respective predetermined times.

[21] The semiconductor integrated circuit of claim 1, wherein:

the first and second port sections and the first and second information holding circuits are formed in a transistor parallel portion including a plurality of transistors arranged in parallel to one another;

the port section and the information holding circuit of a lower operating speed are located in an edge portion of the transistor parallel portion; and

the port section and the information holding circuit of a higher operating speed are located in an inner portion of the transistor parallel portion.

[22] The semiconductor integrated circuit of claim 11, wherein:

the semiconductor integrated circuit includes first and second dummy information holding circuits formed in a cell array in which the first and second information holding circuits are formed; and

the interchange control signal takes into account a interchange time required before information held in the first and second dummy information holding circuits are actually interchanged with each other, and an output of the interchange control signal is stopped after elapse of the interchange time.

[23] The semiconductor integrated circuit of claim 1, wherein a substrate in which the first port section is formed is separated from a substrate of the second port section.

[24] The semiconductor integrated circuit of claim 1, wherein a substrate in which the first information holding circuit is formed is separated from a substrate of the second information holding circuit.

[25] The semiconductor integrated circuit of claim 10, wherein the temporary holding circuit is formed by a transistor circuit, and a threshold value of transistors forming the transistor circuit is set to a threshold value according to an access frequency of the interchange control signal.

[26] The semiconductor integrated circuit of claim 10, wherein a power source voltage supplied to the temporary holding circuit is set to a voltage according an access frequency of the interchange control signal.

[27] The semiconductor integrated circuit of claim 4, wherein:

an access speed of the first and second port sections is a predetermined speed; and

an access frequency of the port section of a lower power source voltage is higher than that of the port section of a higher power source voltage.

[28] The semiconductor integrated circuit of claim 8, wherein an access frequency of the information holding circuit of a lower power source voltage is higher than that of the information holding circuit of a higher power source voltage.

[29] The semiconductor integrated circuit of claim 8, wherein:

a power source voltage of the interchange circuit is higher than that of the information-inputting port section of a lower power source voltage; and

the interchange circuit includes a latch circuit for temporarily holding information held in the information holding circuit connected to the information-inputting port section of a higher power source voltage and outputting the held information to the

information holding circuit connected to the information-inputting port section of a lower power source voltage.

[30] The semiconductor integrated circuit of claim 10, wherein:

the temporary holding circuit is formed by a first inversion circuit and a second inversion circuit;

an output of the first inversion circuit is connected to an input of the second inversion circuit;

the second inversion circuit includes first and second NMOS transistors connected in series with each other;

an input of the first inversion circuit is connected to an output of a first information-inputting port section, an output of a second information-inputting port section, and a drain of a first NMOS transistor of the second inversion circuit;

the first NMOS transistor of the second inversion circuit has a gate connected to an output of the first inversion circuit and a source connected to a drain of the second NMOS transistor; and

an output from the first or second information-inputting port section is input to a gate of the second NMOS transistor of the second inversion circuit.

[31] The semiconductor integrated circuit of claim 30, wherein:

the number of the first or second information-inputting port sections is one; and

a source of the second NMOS transistor of the second inversion circuit receives an inverted signal of a signal from the first or second information-inputting port section.

[32] The semiconductor integrated circuit of claim 30, wherein:

the number of the first or second information-inputting port sections is more than one;

the number of the second NMOS transistors of the second inversion circuit is equal to the number of the first or second port sections;

the plurality of second NMOS transistor are connected in series with one another, and a source of one of the second NMOS transistors that is farthest away from the first NMOS transistor of the second inversion circuit is grounded; and

a gate of each of the plurality of second NMOS transistors receives a signal from a corresponding one of the first or second port sections.

[33] The semiconductor integrated circuit of claim 32, wherein a signal from one of the first or second information-inputting port sections that has a high activity rate is input to a gate of the second NMOS transistor that is farthest away from the first NMOS transistor of the second inversion circuit.

[34] The semiconductor integrated circuit of claim 1, comprising:

a first dummy circuit for reading data from the first information holding circuit and then writing data thereto, and performing a data interchange operation between the first and second information holding circuits; and

a second dummy circuit for reading data from the second information holding circuit and then writing data thereto, and performing a data interchange operation between the first and second information holding circuits, wherein:

a plurality of MOS transistors of the first dummy circuit all have the same MOS property, the MOS property being a diffusion layer concentration, a substrate voltage or a gate oxide film;

some of a plurality of MOS transistors of the second dummy circuit have the same MOS property as that of the MOS transistors of the first dummy circuit, and the other MOS transistors of the second dummy circuit have a MOS property different from that of the MOS transistors of the first dummy circuit;

the semiconductor integrated circuit comprises a power source voltage

adjustment circuit for adjusting power source voltages supplied to the first and second dummy circuits, wherein:

the power source voltage adjustment circuit adjusts the power source voltage value for the first dummy circuit so as to control a delay value of an output signal from the first dummy circuit to a predetermined first reference delay value, and supplies the adjusted power source voltage value to some of the MOS transistors of the second dummy circuit having the same MOS property as that of the first dummy circuit; and

the power source voltage adjustment circuit adjusts the power source voltage value for some of the MOS transistors of the second dummy circuit having a MOS property different from that of the MOS transistors of the first dummy circuit so as to control a delay value of an output signal from the second dummy circuit to a predetermined second reference delay value.

[35] The semiconductor integrated circuit of claim 1, wherein:

the first and second port sections and the first and second information holding circuits are each formed by a transistor circuit;

a group including the first port section and the first information holding circuit and a group including the second port section, the second information holding circuit and the interchange circuit each have a power source voltage supply circuit for supplying a power source voltage of a different value; and

a power source voltage value of the power source voltage supply circuit of each group is set to such a power source voltage value that a total sum of an information read time, an information write time and an information interchange time in a port section of the group is equal to a predetermined time.

[36] The semiconductor integrated circuit of any one of claims 1 to 35, wherein the semiconductor integrated circuit is a multi-thread processor.